WHAT IS CLAIMED IS:

1. A semiconductor package comprising:

at least one leadframe including:

a die paddle having an opening formed therein; and

a plurality of leads, at least one of the leads being disposed in spaced relation to the die paddle, with the remaining leads being attached to the die paddle and extending therefrom;

at least one semiconductor die having a source terminal electrically connected to the die paddle, a gate terminal electrically connected to the at least one of the leads disposed in spaced relation to the die paddle, and a drain terminal; and

a package body at least partially encapsulating the die paddle, the leads, and the semiconductor die such that portions of the leads and the drain terminal of the semiconductor die are exposed in the package body.

2. The semiconductor package of Claim 1 wherein:

the die paddle defines opposed, generally planar top and bottom surfaces; and

the source terminal of the semiconductor die is electrically connected to the bottom surface of the die paddle such that the gate terminal is aligned with and exposed within the opening.

3. The semiconductor package of Claim 2 wherein the at least one lead disposed in spaced relation to the die paddle is electrically connected to the gate terminal of the semiconductor die via a conductive wire which is encapsulated by the package body.

4. The semiconductor package of Claim 2 wherein:

the package body defines a generally planar bottom surface and a side surface;

the leads each define opposed top and bottom surfaces;

the drain terminal of the semiconductor die is exposed in and substantially flush with the bottom surface of the package body;

portions of the leads protrude from the side surface of the package body; and

the exposed portions of the leads are bent such that at least portions of the bottom surfaces thereof extend in generally co-planar relation to the bottom surface of the package body.

5. The semiconductor package of Claim 4 wherein:

the die paddle has a generally quadrangular configuration defining an opposed pair of peripheral edge segments; and

the leads of the leadframe which are attached to the die paddle are segregated into two sets which extend from respective ones of the opposed peripheral edge segments of the die paddle.

6. The semiconductor package of Claim 4 wherein:

the die paddle has a generally quadrangular configuration defining at least four peripheral edge segments; and

the leads of the leadframe are disposed along a common one of the peripheral edge segments of the die paddle.

7. The semiconductor package of Claim 2 wherein:

the package body defines a generally planar bottom surface;

each of the leads defines opposed top and bottom surfaces;

the drain terminal of the semiconductor die is exposed within and substantially flush with the bottom surface of the package body; and

at least a portion of the bottom surface of each of the leads is exposed in and substantially flush with the bottom surface of the package body.

8. The semiconductor package of Claim 7 wherein:

the die paddle has a generally quadrangular configuration defining an opposed pair of peripheral edge segments; and

the leads of the leadframe are segregated into two sets which are disposed along respective ones of the opposed peripheral edge segments of the die paddle.

9. The semiconductor package of Claim 8 wherein each of the leads of one of the sets is disposed in spaced relation to the die paddle, with at least one of the leads of the remaining set being disposed in spaced relation to the die paddle.

10. The semiconductor package of Claim 7 wherein:

the die paddle has a generally quadrangular configuration defining at least four peripheral edge segments; and

the leads of the leadframe are disposed along a common one of the peripheral edge segments of the die paddle.

11. The semiconductor package of Claim 7 wherein:

the die paddle has a generally quadrangular configuration defining at least four peripheral edge segments; and

the leads of the leadframe are disposed along each of the peripheral edge segments of the die paddle.

12. The semiconductor package of Claim 7 wherein each of the leads includes a half-etched portion which is encapsulated by the package body.

13. The semiconductor package of Claim 2 wherein:

the package body defines opposed, generally planar top and bottom surfaces;

the drain terminal of the semiconductor die is exposed within and substantially flush with the bottom surface of the package body; and

the top surface of the die paddle is exposed within and substantially flush with the top surface of the package body.

14. The semiconductor package of Claim 2 wherein:

the die paddle has a generally quadrangular configuration defining at least four corner regions; and

the opening comprises a notch formed within one of the four corner regions of the die paddle.

15. The semiconductor package of Claim 2 wherein the opening comprises an aperture disposed within the die paddle.

16. The semiconductor package of Claim 1 wherein the die paddle is sized and configured relative to the semiconductor die such that the gate terminal of the semiconductor die is not covered by the die paddle and thus exposed when the source terminal is electrically connected to the die paddle.

17. A semiconductor package comprising:

a leadframe including:

a die paddle having an opening formed therein; and

a plurality of leads, at least one of the leads being disposed in spaced relation to the die paddle, with the remaining leads being attached to the die paddle and extending therefrom;

a semiconductor die having a source terminal electrically connected to the die paddle, a gate terminal electrically connected to the at least one of the leads

disposed in spaced relation to the die paddle, and a drain terminal; and

a layer of encapsulant partially encapsulating the die paddle, the leads, and the semiconductor die.

18. The semiconductor package of Claim 17 wherein:

the die paddle defines opposed, generally planar top and bottom surfaces; and

the source terminal of the semiconductor die is electrically connected to the bottom surface of the die paddle such that the gate terminal is aligned with and exposed within the opening.

19. The semiconductor package of Claim 18 wherein the at least one lead disposed in spaced relation to the die paddle is electrically connected to the gate terminal of the semiconductor die via a conductive wire which is encapsulated by the encapsulant layer.

20. The semiconductor package of Claim 18 wherein:

the die paddle has a generally quadrangular configuration defining at least four peripheral edge segments; and

the leads of the leadframe are disposed along a common one of the peripheral edge segments of the die paddle.

21. The semiconductor package of Claim 1, further comprising:

a second leadframe including:

a second die paddle having an opening formed therein; and

a plurality of second leads, at least one of the second leads being disposed in spaced relation to the second die paddle, with the remaining second leads being attached to the second die paddle and extending therefrom;

a second semiconductor die having a source terminal electrically connected to the second die paddle, a gate terminal electrically connected to the at least one of the second leads disposed in spaced relation to the second die paddle, and a drain terminal;

the package body further at least partially encapsulating the second die paddle, the second leads, and the second semiconductor die such that portions of the second leads and the drain terminal of the second semiconductor die are exposed in the package body.